

WHAT IS CLAIMED IS:

1 1. A radio frequency (RF) down/up-conversion circuit
2 comprising:

3 a local oscillator chopping circuit comprising:

4 a frequency divider circuit capable of receiving
5 a first local oscillator (LO) signal having a frequency of
6 LO and generating therefrom a frequency-divided second
7 local oscillator (LO) signal having a frequency of LO/N and
8 synchronized with said first LO signal; and

9 a multiplier capable of receiving said first and
10 second LO signals and generating a product signal of said
11 first and second LO signals; and

12 a differential radio frequency (RF) mixer having a
13 first differential input port capable of receiving said product
14 signal from said multiplier and a second differential input port
15 capable of receiving a first differential modulated radio
16 frequency (RF) signal and a second differential modulated radio
17 frequency (RF) signal, wherein said differential RF mixer
18 generates a differential output signal.

1 2. The radio frequency down/up-conversion circuit as set
2 forth in Claim 1 wherein said multiplier is an analog multiplier.

1 3. The radio frequency down/up-conversion circuit as set
2 forth in Claim 1 wherein said multiplier is an exclusive-OR gate.

1 4. The radio frequency down/up-conversion circuit as set
2 forth in Claim 1 wherein said differential output signal of said
3 differential RF mixer is a double-sideband suppressed carrier
4 signal.

1 5. The radio frequency down/up-conversion circuit as set
2 forth in Claim 4 further comprising a chopping switch capable of
3 receiving said differential output signal of said differential RF
4 mixer.

1 6. The radio frequency down/up-conversion circuit as set
2 forth in Claim 5 wherein said chopping switch is synchronized to
3 said frequency divider such that said switching switch switches
4 its internal connections at said LO/N frequency of said frequency
5 divider and in tandem with said frequency divider.

1 7. The radio frequency down/up-conversion circuit as set
2 forth in Claim 1 wherein said differential RF mixer comprises a
3 first differential pair of transistors comprising a first
4 transistor and a second transistor, wherein a base of said first
5 transistor is coupled to a first differential output signal
6 received from said multiplier, and an emitter of said first
7 transistor is coupled to an emitter of said second transistor and
8 to said first differential modulated radio frequency (RF) signal.

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1 8. The radio frequency down/up-conversion circuit as set
2 forth in Claim 7 wherein said differential RF mixer comprises a
3 second differential pair of transistors comprising a third
4 transistor and a fourth transistor, wherein a base of said third
5 transistor is coupled to a second differential output signal
6 received from said multiplier, and an emitter of said third
7 transistor is coupled to an emitter of said fourth transistor and
8 to said second differential modulated radio frequency (RF)
9 signal.

1 9. The radio frequency down/up-conversion circuit as set
2 forth in Claim 8 wherein a collector of said first transistor is
3 coupled to a collector of said third transistor to form a first
4 differential output signal of said differential output signal
5 generated by said RF mixer and wherein a collector of said second
6 transistor is coupled to a collector of said fourth transistor to
7 form a second differential output signal of said differential
8 output signal generated by said RF mixer.

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10. A radio frequency (RF) receiver comprising:
a receiver front-end circuit capable of receiving an incoming RF signal from an antenna and filtering and amplifying said incoming RF signal; and
a radio frequency (RF) down/up-conversion circuit coupled to said receiver front-end circuit comprising:
a local oscillator chopping circuit comprising:
a frequency divider circuit capable of receiving a first local oscillator (LO) signal having a frequency of LO and generating therefrom a frequency-divided second local oscillator (LO) signal having a frequency of LO/N and synchronized with said first LO signal; and
a multiplier capable of receiving said first and second LO signals and generating a product signal of said first and second LO signals; and
a differential radio frequency (RF) mixer having a first differential input port capable of receiving said product signal from said multiplier and a second differential input port capable of receiving a first differential modulated radio frequency (RF) signal and a second differential modulated radio frequency (RF) signal, wherein said differential RF mixer generates a differential output signal.

1 11. The radio frequency receiver as set forth in Claim 10
2 wherein said multiplier is an analog multiplier.

1 12. The radio frequency receiver as set forth in Claim 10
2 wherein said multiplier is an exclusive-OR gate.

1 13. The radio frequency receiver as set forth in Claim 10
2 wherein said differential output signal of said differential RF
3 mixer is a double-sideband suppressed carrier signal.

1 14. The radio frequency receiver as set forth in Claim 13
2 further comprising a chopping switch capable of receiving said
3 differential output signal of said differential RF mixer.

1 15. The radio frequency receiver as set forth in Claim 14
2 wherein said chopping switch is synchronized to said frequency
3 divider such that said switching switch switches its internal
4 connections at said LO/N frequency of said frequency divider and
5 in tandem with said frequency divider.

1 16. The radio frequency receiver as set forth in Claim 10
2 wherein said differential RF mixer comprises a first differential
3 pair of transistors comprising a first transistor and a second
4 transistor, wherein a base of said first transistor is coupled to
5 a first differential output signal received from said multiplier,
6 and an emitter of said first transistor is coupled to an emitter
7 of said second transistor and to said first differential
8 modulated radio frequency (RF) signal.

1 17. The radio frequency receiver as set forth in Claim 16
2 wherein said differential RF mixer comprises a second
3 differential pair of transistors comprising a third transistor
4 and a fourth transistor, wherein a base of said third transistor
5 is coupled to a second differential output signal received from
6 said multiplier, and an emitter of said third transistor is
7 coupled to an emitter of said fourth transistor and to said
8 second differential modulated radio frequency (RF) signal.

1 19. A method of demodulating an incoming differential radio
2 frequency (RF) signal having a frequency of RF comprising the
3 steps of:

4 receiving a first local oscillator (LO) signal having a
5 frequency of LO;

6 generating therefrom a frequency-divided second local
7 oscillator (LO) signal having a frequency of LO/N and
8 synchronized with the first LO signal;

9 multiplying the first and second LO signals and
10 generating a product signal of the first and second LO signals;
11 and

12 mixing the product signal from the multiplier and the
13 differential radio frequency signal and generating a differential
14 output signal.

15
16 20. The method as set forth in Claim 19 wherein the
17 differential output signal is a double-sideband suppressed
18 carrier signal.